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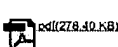
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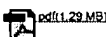
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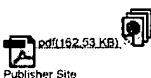
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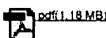
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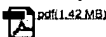
**5** [The Kiewit network: a large AppleTalk internetwork](#)

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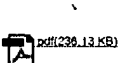
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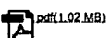
**7** [The NuMesh: a modular, scalable communications substrate](#)

Steve Ward, Karim Abdalla, Rajeev Dujari, Michael Fetterman, Frank Honoré, Ricardo Jenez, Philippe Laffont, Ken Mackenzie, Chris Metcalf, Milan Minsky, John Nguyen, John Pezaris, Gill Pratt, Russell Tessier

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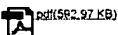
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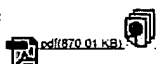


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A. Hein, J. Dalcolmo, P. Le Corre, R. Lauwereins, M. Adé  
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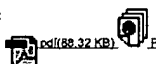
<sup>10</sup> Hardware/software co-simulation in a VHDL-based test bench approach

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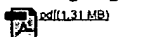
<sup>11</sup> Enhanced code compression for embedded RISC processors

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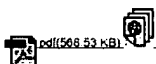
<sup>12</sup> Synthesis of multi-rate and variable rate circuits for high speed telecommunications applications

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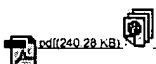
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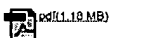
<sup>14</sup> A real-time assistive computer interface for users with motor disabilities

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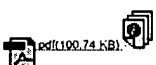
<sup>15</sup> A generic architecture for on-chip packet-switched interconnections

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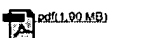
<sup>16</sup> An overview of portable GUI software

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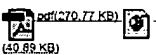
<sup>17</sup> Proactive computing

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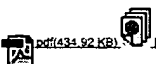
<sup>18</sup> A hierarchical functional structuring and partitioning approach for multiple-FPGA implementations

Wen-Jong Fang, Allen C.-H. Wu

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<sup>9</sup> A register file and scheduling model for application specific processor synthesis

E. Ercanli, C. Papachristou

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Ehitajate tee 5, EE-0026 Tallinn, Estonia raiub@pld.ttu.ee. Test Synthesis with Alternative Graphs  
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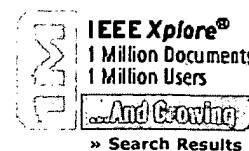
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 Pages:1 - 466

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*Higuchi, T.; Iwata, M.; Keymeulen, D.; Sakanashi, H.; Murakawa, M.; Kajitani, I.; Takahashi, E.; Toda, K.; Salami, N.; Kajihara, N.; Otsu, N.;*

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**12 Design and implementation of an FPGA-based control IC for AC-voltage regulation**

*Shih-Liang Jung; Meng-Yueh Chang; Jin-Yi Jyang; Li-Chia Yeh; Ying-Yu Tzou;*

Power Electronics, IEEE Transactions on , Volume: 14 , Issue: 3 , May 1999

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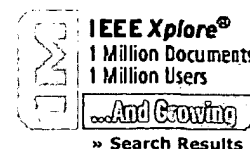
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